# Control signals

For this single cycle processors, there are totally seven control signals need to be designed and assignment: regWr, regDst, branch, extOp, ALUSrc, MemWr and memToReg.

And this processor need to implement fifteen functions: Add, Addi, Addu, Sub, Subu, And, Or, Sll, Lw, Sw, Beq, Bne, Bgtz, Slt and Sltu.

After analysing the relationship between control signals and the specific implemented function, the below table has been given, which give a list that when a function need to be implemented, the control signal must be set to 1:

|  |  |
| --- | --- |
| regWr | Add, addu, sub, subu, slt, sltu, and, or, sll, lw, addi |
| regDst | Add, addu, sub, subu, slt, sltu, and, or, sll, addi |
| Branch | Beq, bne, bgtz |
| extOp | Lw, sw, addi |
| ALUSrc | Lw, sw, addi, sll |
| memWr | Sw |
| memToReg | lw |

**Table 1: The specific functions when a control signal must be set to 1**

(这里要不要解释一下为什么不需要考虑Jump和ALUctr).

